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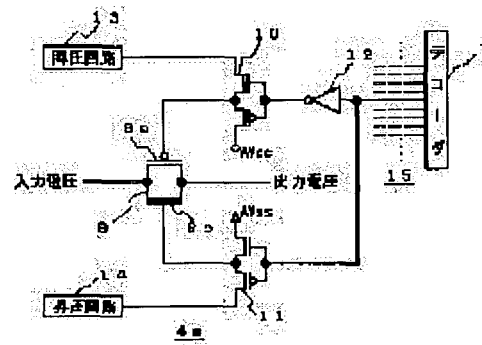
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(54) SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:

PURPOSE: To improve the conversion accuracy of a D/A converter by lowering the gate voltage of the p-type MOS of a CMOS analog switch in a voltage lowering circuit and raising the gate potential of an n-type MOS in a boosting circuit.

CONSTITUTION: A CMOS transmission gate 4a is composed of the CMOS analog switch 9 for which the p-type and n-type MOSes 9a and 9b are parallelly connected, an inverter 10 for which resistor decoder 7 are inputted and the output is connected to the gate inverter 12 and output is connected to the gate electrode of the p-type MOS 9a and the inverter 11 for which signals from the decoder 7 are inputted and the output is connected to the gate electrode of the n-type MOS 9b. Then, the voltage lowering circuit 13 is connected to the grounded electrode side of the p-type MOS 9a and the gate potential of the p-type MOS 9a is lowered at the time of the operation of the CMOS analog switch 9. Also, the boosting circuit 14 is connected to the power supply electrode side of the n-type MOS 9b and the gate potential of the n-type MOS 9b is raised at the time of the operation of the CMOS analog switch 9.



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